Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OFFSET N1**
2. **IN –**
3. **IN +**
4. **GND**
5. **OFFSET N2**
6. **OUT**
7. **VDD**
8. **BIAS SELECT**

**2 1 8 7**

**3 4 5 6**

**.048”**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Ground**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .048” X .055” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: TLC271AM**

**DG 10.1.2**

#### Rev B, 7/19/02